A High-Power Millimeter-Wave Frequency Doubler Using a Planar Diode Array

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***Abstract*—A balanced frequency doubler has been built using an integrated planar array of four varactor diodes. The maximum output power of 55 mW at 174 GHz is twice the power available from the previous best multiplier at a nearby frequency and was limited by the available pump source. The peak efficiency is 25% at 150 mW input. Circuit parasitics and device heating do not appear to be significant at the present power levels and carrier velocity saturation effects appear to be reduced due to the series array configuration.**

I. Introduction

IN THE FREQUENCY RANGE above 100 GHz, frequency multipliers can achieve high conversion efficiency at low input power, but tend to saturate in output at a rather low power level. This saturation is believed to be due to the finite maximum carrier velocity in the GaAs epitaxial layer [1], which limits the displacement current in the varactor. This causes the efficiency to decrease rapidly above a critical power, rather than increasing to the reverse breakdown limit. Since the current increases with frequency for a given voltage swing, this becomes a major limitation for submillimeter applications. Because the saturated carrier velocity is not easily increased, the only alternative is to decrease the current density, through the use of several diodes or diodes with a larger area. One partial solution has been to build balanced doublers using a pair of whiskered diodes [2], but this is not extendible to larger numbers of diodes.

The use of series arrays of diodes is an attractive approach because it allows one to increase both the area and the number of diodes, while they may be treated as a single diode as far as circuit design is concerned. Also, a series array of n identical diodes of individual area nA, behaves the same as an $n \times n$ array of similar diodes of individual area A. Thus, the series array can handle n^2 times the amount of power as a single diode (of area A), without increasing the current density or changing the total impedance level. While series arrays are quite impractical using whiskered diodes, they are readily fabricated using planar technology. The doubler described in this work, operating with an output frequency near 170 GHz, uses four planar diodes fabricated on a single chip.

Manuscript received February 19, 1993. This work was supported by NASA through Grants GSRP-4979-91, NAGW-2377, and NAGW-2430 and through the JPL Grants 958202 and 959189.

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IEEE Log Number 9209406.

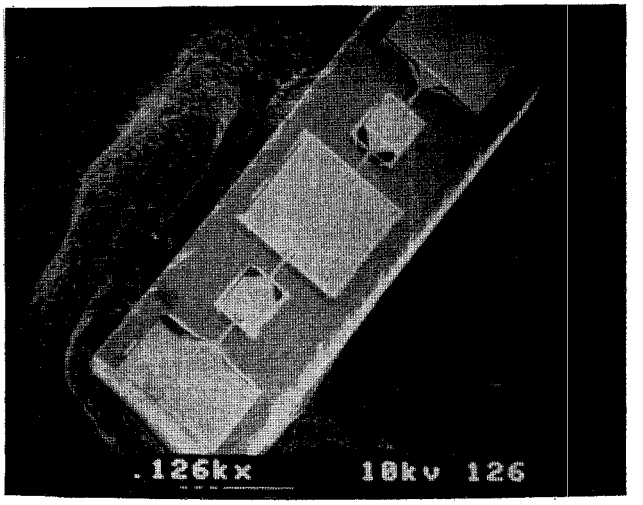

Fig. 1. SEM photograph of the balanced doubler chip.

It produces twice the output power of a two diode whisker-contacted doubler at a similar frequency, clearly demonstrating the potential for such arrays.

II. Diode Design Goals and Fabrication

The circuit is based on the balanced doubler of Erickson [4]. Thus an initial constraint was that the chip fit into this multiplier. The chip has four diodes laid out as a linear array consisting of two pairs, shown in Fig. 1. The large central pad serves as the ohmic contact for the two central diodes, as well as the output bonding pad. The ohmic contacts for the end diodes are the two small inner pads. The end pads are sized to permit the chip to be soldered to the top and bottom walls of the waveguide. The length of the inductive "fingers" was maximized, within the other constraints, to improve the matching to the varactor capacitance.

The junction capacitance of each anode was chosen so that each series pair had the same capacitance as the single whiskered diodes used by Erickson [2], about 20 fF. Since current saturation is believed to be the major limitation on the maximum input power, the breakdown voltage was considered less important. In fact, the most successful planar diode batch had an increased epitaxial layer doping to reduce series resistance at the cost of lower breakdown voltage.

The diode fabrication followed the surface channel process, [3]–[5], except for a few modifications. Specifically, the SC10V2 diodes included N^+ InGaAs and GaAs layers covering the n-type GaAs active layer. These layers were used

TABLE I
BALANCED DOUBLER CHIP CHARACTERISTICS

Batch #	t_{chip} (μm)	t_{epi} (μm)	N_{epi} (cm^{-3})	diam. (μm)	Single Anode		
					C_{jo} (fF)	R_s (Ω)	V_b (V)
SC10T1	100	1.3	1.8×10^{16}	10	33	12	22
SC10T2	100	1.2	2.5×10^{16}	10	40	7	17
SC10V1	100	0.64	4.5×10^{16}	10	50	3	15
SC10V2	25	0.64	4.5×10^{16}	9	38	6	15

to achieve a lower ohmic contact resistance. The fabrication process was modified to include removal of these layers from the anode region of the chip before the silicon dioxide layer, which defines the anode, was deposited. Four batches of balanced doubler chips were fabricated and their physical and electrical characteristics are given in Table I.

III. DC DEVICE CHARACTERISTICS

The small signal resistance of the best diodes (SC10V2) was measured in the doubler mount using a vector network analyzer at 130 MHz to avoid errors due to heating effects at dc [6]. Data was taken over a range of currents up to 50 mA, and the series resistance was fitted after correction for the exponential slope of the ideal junction. The best fit value was 6.2 Ω per anode, while dc measurement yielded a value of 5.2 Ω.

The capacitance of each junction was measured at 4–10 GHz using a transmission measurement between two wafer probes. A chip with broken anode fingers showed a pad-to-pad capacitance of 9.7 fF for the two end diodes and 11 fF for the central diodes. An additional capacitance of 2 fF was found between the center pad and each of the end pads. The remaining capacitance, assumed to be that of the junction, is 38 ± 1 fF. The CV data can be fitted by a $\gamma = 0.4$ law assuming no additional parasitic contributions, or by a $\gamma = 0.5$ law if one assumes that 4 fF of parasitic capacitance is found close to the anode (however, this is much larger than the 1–1.5 fF that we estimate for the finger structure).

IV. DOUBLER MOUNT AND RF EVALUATION

The doubler mount is electrically equivalent to that in [2], but was redesigned for use with planar diodes, Fig. 2. All the waveguides were milled symmetrically about the center line with the coaxial sections milled with a square outer section. The diode is soldered to the waveguide top and bottom walls as well as to the center pin in one operation. The chip is supported by the solder joints, and the resulting structure is quite robust.

A klystron oscillator at 87 GHz was used to determine the performance of the SC10V2 diodes. For these tests, the input and output match were optimized using teflon quarter-wave transformers positioned in the waveguide so that the output power was maximized. The input reflected power measured with a coupler was 8% at the maximum input power. The bias was 12 V with 0.5 mA forward current. Data for the power output and efficiency vs. input power, with the bias optimized

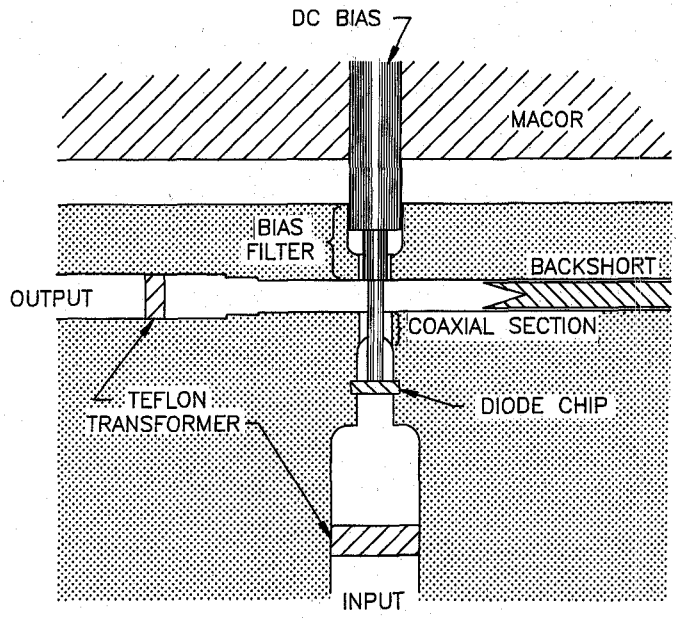

Fig. 2. A cross section through the doubler block.

at each point, are shown in Fig. 3. The efficiency peaks at 25% with 150 mW input. The peak output power is 55 mW at an estimated input power of 250 mW (all other input powers were measured with a directional coupler which was removed for this final test). Input and output power calibrations were obtained with the same calorimeter built in WR-12 waveguide [7]. This output power is over a factor of two higher than the previous best doubler at a nearby frequency.

The theoretical efficiency of the diode array, as calculated by a standard multiplier analysis program [8] and assuming $\gamma = 0.4$, is 35% at an input power of 160 mW, which implies 1.5-dB loss within the doubler block. This is about 0.5 dB more than is expected, and may suggest the amount by which current saturation reduces the efficiency.

The quality of the impedance match that was achieved with the 25-μm thick SC10V2 chips is comparable to that with whiskered diodes in the comparable mount. However, the match achieved with diodes on 100 μm substrates is much worse.

V. CONCLUSION

We have demonstrated the first application of a planar series array of varactor diodes in the mm-wave range, and have achieved the highest output power from a frequency doubler near 170 GHz. The saturation velocity effects that limit

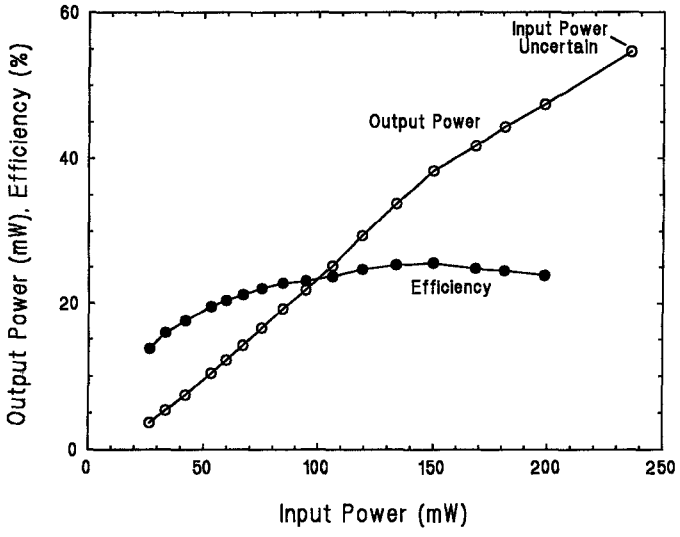

Fig. 3. Output power and efficiency versus input power for the balanced doubler at 87 GHz input.

GaAs varactor diode performance above 100 GHz appear to be significantly reduced in the series diode structure. Higher efficiency should be obtainable with this type of diode if the doping density is increased to reduce series resistance at the expense of slightly reduced breakdown voltage. These results are particularly important because for the first time a planar Schottky device has displayed significantly superior performance to its whisker-contacted counterpart, demonstrating the potential of the planar technology in general and of the series varactor arrays in particular.

ACKNOWLEDGMENT

The authors thank M. Zybura and Dr. S. Jones of the University of Virginia for supplying the InGaAs epitaxial wafers.

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